VIGNAN'S
Foundation for Science, Technology & Research
UNIVERSITY
(Estd u/s 3 of UGC Act of 1956)

Department of Electronics and Communication Engineering

Date: **13.07.2017**

Minutes of the Board of studies (BOS) meeting for MTech VLSI(VT) held on13.07.2017in SRAVANTHI Seminar hall.

The following are the members presented for the meeting.

1) Dr.N.V.S.N.Sharma - External member from NIT-Warangal
2) Dr. G.Srinivasulu - External member from SVU College of Engineering.
3) Dr. B. Seetharamanjaneyulu. - Professor, ECE
4) Dr. N. Usha Rani - Professor & HOD,ECE
5) Mrs.M.Sarada - Assistant Professor

The following views were expressed by the external members

- The syllabus is accepted by majority of members - however the following observations are made to improve core competence in VLSI Design.
- It is suggested by all the members to increase number of electives (i.e. minimum of 15 electives)
- In the courses VLSI technology and VLSI Testing and Validation, it is suggested that to add one more credit for the practical as a capston project.
- Two to three electives can be added by choosing subjects from Embedded Systems/DCN specialization.
- For VLSI Signal processing, SOC, ASIC subjects, it is suggested that to add detailed contents in the syllabus.
- All BoS members suggested to modify and design Skills acquired and Activities dynamically time to time.
- It is suggested to add NPTEL/Coursera/edX videos/courses as a reference correspond to the subjects
- Workshop on Technical English is suggested for all P.G students

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Outcomes:

1. BOS members approved the revised curriculum (Structure, Syllabus and regulations) of MTech VLSI and it follows Choice Based Credit System . Course Structure is provided in Appendix I.
2. Major restructuring has taken place in the Curriculum with theory courses integrated with laboratory sessions.
3. All the Courses in the Curriculum are designed to fall under either of the domains of employability (or) skill development (or) Entrepreneurship. The mapping of the courses with employability or skill development is provided in Appendix II.
4. In all the courses of the revised curriculum (R17) substantial changes are made in the content. The percentage of revision from R14 - R17is 25%.
5. Stakeholders feedback is collected, analyzed, and given utmost priority while designing the curriculum and their suggestions are implemented.
6. The finalized Course Structure is shown in Appendix II and III

Appendix I
Course Structure -MTech (VLSI)
2017 Regulation

I Year - I Semester

Course Code	Course Title	L	T	P	C
Professional Core	Analog IC Design	3	-	3	5
Professional Core	Digital IC Design	3	-	3	5
Professional Core	VLSI Technology	4	-	-	4
Professional Core	Semiconductor Device Modeling	3	1	-	4
			Total Core Credits		**18**

I Year - II Semester

Course Code	Course Title	L	T	P	C
Professional Core	Mixed Signal Design	3	-	3	5
Professional Core	VLSI Testing and Validation	4	-	-	4
Professional Core	Low power VLSI Design	3	1	-	4
Professional Core	Modelling and Synthesis with Verilog HDL	3	-	3	5
Employability	Research Methods	3	-	-	3
Employability	Employment Orientation Program	2	-	-	2
Total Semester Credits					**23**

II Year- I & II Semesters

Course Code	Course Title	L	T	P	C
	I Semester				
Core	Project/ Internship Phase - I				15
	II Semester				
Core	Project/ Internship Phase - II				15

Pool of Electives

Course Code	Course Title	L	T	P	C
Elective	Scripting languages	3	1	2	5
Elective	VLSI Signal Processing	3	1	-	4
Elective	Verification Methodologies	4	-	-	4
Elective	System On-chip Design	4	-	-	4
Elective	CAD VLSI	3	1	-	4
Elective	Advanced digital system design	3	1	-	4
Elective	Nano Electronics	4	-	-	4
Elective	ASIC	4	-	-	4
Electives	MEMS	3	1	-	4
Electives	Semiconductor Memory Design	4	-	-	4
Electives	Nano Sensors and its Applications	4	-	-	4
Electives	RF integrated circuit design	3	1	-	4

Note : The courses that are highlighted denote implementation of " Choice Based Credit System(CBCS)"

Signature of BOS Chairman

APPENDIX – II

List of courses that enable employability or entrepreneurship or skill development in the R-17 MTech – VLSI

Sl.	Course Name	Core / Elective	Year	Employability / Skill Development/Entrepreneurship
1	Analog IC Design	Core	I	Skill Development
2	Digital IC Design	Core	I	Skill Development
3	VLSI Technology	Core	I	Skill Development
4	Semiconductor Device Modeling	Core	I	Employability
5	Mixed Signal Design	Core	I	Skill Development
6	VLSI Testing and Validation	Core	I	Employability
7	Low power VLSI Design	Core	I	Skill Development
8	Modelling and Synthesis with Verilog HDL	Core	I	Skill Development
9	Scripting languages	Elective	I	Skill Development
10	VLSI Signal Processing	Elective	I	Skill Development
11	Verification Methodologies	Elective	I	Skill Development
12	System On-chip Design	Elective	I	Employability

13	CAD VLSI	Elective	I	Employability
14	Advanced digital system design	Elective	I	Skill Development
15	Nano Electronics	Elective	I	Skill Development
16	ASIC	Elective	I	Skill Development
17	MEMS	Elective	I	Employability
18	Semiconductor Memory Design	Elective	I	Employability
19	Nano Sensors and its Applications	Elective	I	Skill Development
20	RF integrated circuit design	Elective	I	Skill Development

Note : The courses that are highlighted denote the implementation of "Choice Based Credit Systemm(CBCS)"

Signature of BOS Chairman

APPENDIX - III
List of new courses in the R-17 Regulations
MTech – VLSI

Sl.	Course Name	Year
1	Analog IC Design	I
2	Digital IC Design	I
3	VLSI Technology	I
4	Semiconductor Device Modeling	I
5	Mixed Signal Design	I
6	VLSI Testing and Validation	I
7	Low power VLSI Design	I
8	Modelling and Synthesis with Verilog HDL	I
9	Scripting languages	I
10	VLSI Signal Processing	I
11	Verification Methodologies	I
12	System On-chip Design	I
13	CAD VLSI	I
14	Advanced digital system design	I
15	Nano Electronics	I
16	ASIC	I
17	MEMS	I
18	Semiconductor Memory Design	I
19	Nano Sensors and its Applications	I
20	RF integrated circuit design	I

Signature of BOS Chairman

The following are the members present for the board of studies meeting held at Department of Electronics &Communication Engineering on 13-07-2017

External Members :

Sl. No.	Name of the Member	Designation	Signature
1.	Dr.N.V.S.N.Sharma	Professor, NIT, Warangal.	
2.	Dr.G.Srinivasulu	SVU College of Engineering.	

Internal Members :

Sl. No.	Name of the Member	Designation	Signature
1.	Dr.B.Seetharamananjaneyalu	Professor	
2.	Dr.N.Usha Rani	Professor & HOD	
3.	Mrs.M.Sarada	Assoc. Professor	

Signature Of BOS Chairman